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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Robert Louis Hodges
Application No.	:	09/733,243
Filed	:	December 7, 2000
For	:	SELF-ALIGNED GATE AND METHOD

Examiner	:	Michael Manh Trinh
Art Unit	:	2822
Docket No.	:	98-P-104C1 (850063.542C1)
Date	:	November 24, 2003

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF (37 C.F.R. § 1.192)

Dear Sirs:

This brief is in furtherance of the Notice of Appeal, filed in this case on June 27, 2003. The fees required under Section 1.17(c), and a request for a three-month extension of time for filing this brief are enclosed with the accompanying fee transmittal. Applicant hereby requests any extension of time necessary for acceptance of this Appeal Brief, and any other fees which may become due, and authorizes said fees be charged to Deposit Account No. 19-1090. This request is made separately in the Petition for Extension of Time for the convenience of the Office.

I. REAL PARTY IN INTEREST

The real party in interest is STMicroelectronics, Inc., which is the current name of the assignee of the present invention. The assignment of record is to SGS-Thomson Microelectronics, Inc., having an address at 1310 Electronics Drive, Carrolton, Texas 75006.

The company underwent an official name change in 1998, but maintained the same corporate identity and ownership of this application. If the Examiner requests, a copy of the official change in name can be provided.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which directly affect or will be directly affected by or have a bearing on the Board's decision in this appeal. This application is a continuation of United States Patent Application No. 09/170,957, filed October 13, 1998, now abandoned.

III. STATUS OF CLAIMS

Claims 14-24 and 26 are currently pending and active in the application. Of these claims, claims 14-24 and 26 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 14, 17, 20, 21, 22, 23 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kao in view of Yu and Hook. Claims 15, 16, 19 and 24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Kao taken with Yu and Hook, as applied to claims 14, 17, 20, 21, 22, 23 and 26, and further of Niwa or Chau. Claim 18 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kao taken with Yu and Hook, as applied to claims 14, 17, 20, 21, 22, 23 and 26, and further of Wolf. Claim 25 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kao taken with Yu and Hook, as applied to claims 14, 17, 20, 21, 22, 23 and 26, and further of Goth. All pending active claims are attached as Appendix A.

IV. STATUS OF AMENDMENTS

The Final Rejection was mailed March 28, 2003. In response to this Final Rejection, a Notice of Appeal has been filed. No amendments after final have previously been filed, nor are

any filed herewith. The claims now pending in the application were those filed in the Amendment dated January 3, 2003.

V. SUMMARY OF INVENTION

The present invention provides for higher density in semiconductor circuits. Cost depends, in part, on how much semiconductor area is required to implement desired functions. A semiconductor made according to principles of the present invention can be made much smaller, and therefore cheaper, than was possible in the prior art.

Semiconductor features made with a mask are generally limited in how small they can be made. The smallest size that can be imaged through a mask is similar to the wavelength of light used to photolithographically define the feature. While modern technology has led to reduction of the size of the smallest mask feature, large capital cost of these processes and machinery make it an inefficient solution. Further, as the size of a semiconductor is reduced, the parasitic capacitance increases. This leads to a decrease in maximum operating frequency, an important figure of merit for integrated circuits.

This invention permits features to be formed in the semiconductor which are smaller than the smallest mask feature and yet have good operating characteristics.

According to principles of the present invention, a layer 52 is deposited on the substrate and a narrow opening 62 is formed between the two layers. The narrow opening 62 will normally be at the smallest dimension possible for the mask and photolithographic dimensions used.

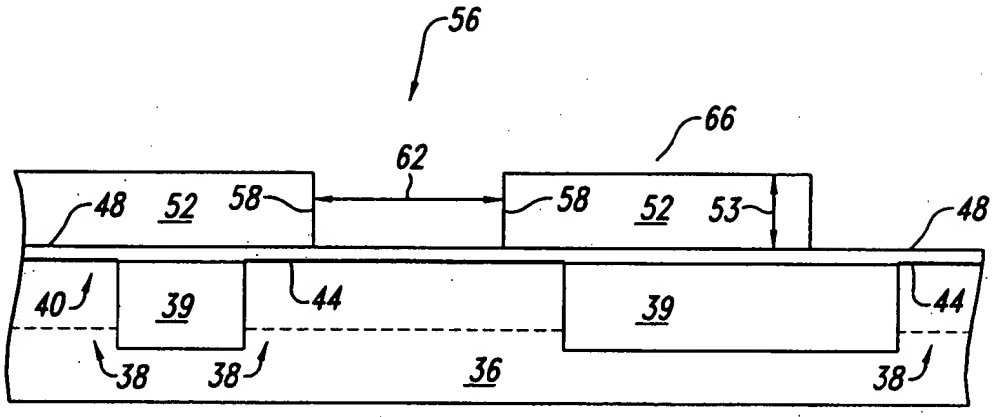


Figure 1 shows Figure 3 of the application as filed

As can be seen in Figure 1 above, the opening 62 is formed in the insulating layer 52.

Sidewall spacers are then formed on the insulating layer 52 making an even more narrow opening 76 having the dimensions 78.

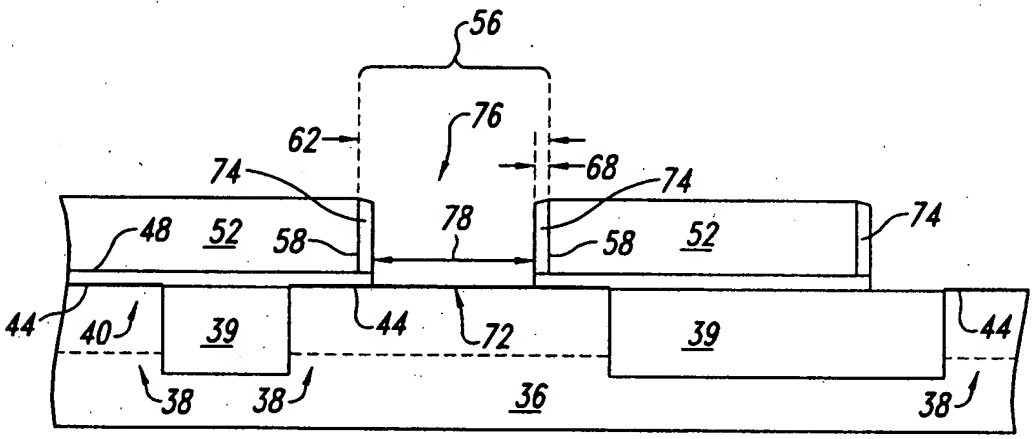


Figure 2 is Figure 5 of the application as filed

A shown in Figure 2 above, the narrow opening 76 is formed because the sidewalls 74 decrease the width of the opening 62. The opening 76 is now the critical dimension which is the smallest dimension which can be formed on the integrated circuit.

According to the embodiment as claimed, an ion implant is now performed at various angles to place a selected doping concentration under the sidewall spacers 74. As stated in the application as filed, page 8, lines 18-25, in this embodiment, implanting is done at multiple

angles to provide halos or pockets of implanted ions under the dielectric spacers 74 on each side of the openings 56 but not in the gaps 76 between the dielectric spacers 74. Namely, the openings 56 do not receive the ion implant because of the selected angle and instead the implant is only performed under the dielectric spacers. This ensures that the threshold voltage at which the device turns on is not affected by the halo implant. Rather, the implant is only done under the sidewall oxides and not underneath the gate electrode itself.

The present invention implements a substrate structure that allows ions to be implanted at an angle to form a pocket and halo of ions beneath the sidewall spacers. The resulting device exhibits a self aligned channel running beneath the opening and pocket/halo extensions from the source and drain residing outside the opening.

The solution according to the present invention can be most easily seen in Figure 7 of the present application, reproduced below for ease of reference.

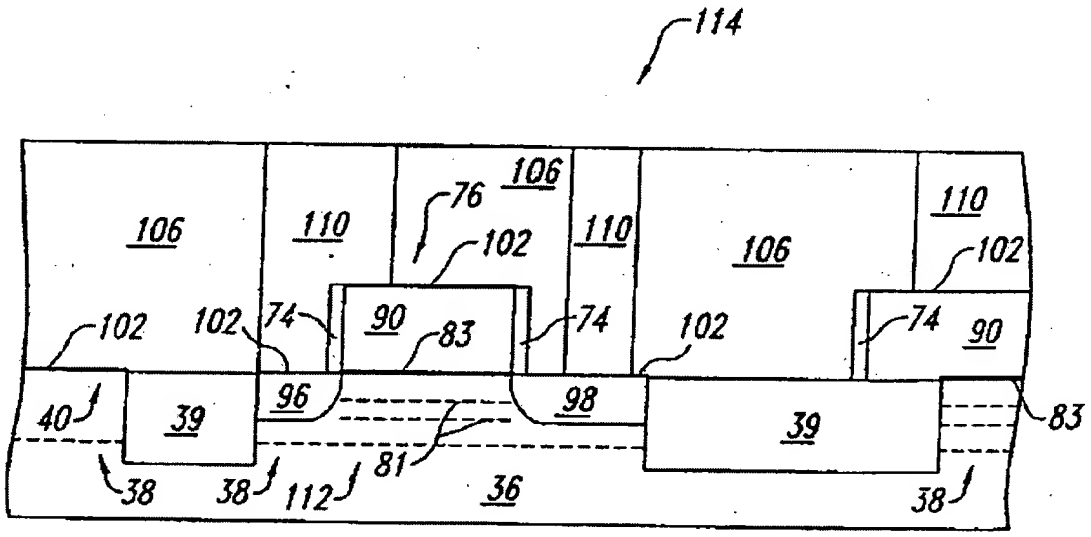


Figure 3 is a copy of Figure 7 of the present application.

As can be seen by viewing Figure 3 above, a channel 81 runs below the gate 90. Source and drain regions 96, 98 reside on either side of gate 90 and can be extended via pocket and halo extensions beneath the sidewall spacers 74. Such pocket/halo extensions can be implanted via small-angle implantation techniques, and are an available solution because of the single dopant-type channel 81 without the existence of a different-type implant region.

The present invention provides for a reduced gate width than was previously available, as well as pocket/halo extensions from the source and drain, to reside below sidewall spacers. This reduces the parasitic capacitance otherwise prevalent in a device with such a small gate opening, and therefore provides for increased maximum operating frequency. Furthermore, semiconductors manufactured according to this method are much smaller, and therefore cheaper to produce.

VI. ISSUES

1. Whether claims 14, 17, 20, 21, 22, 23 and 26 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 5,688,700 to Kao et al. taken with U.S. Patent No. 6,190,980 to Yu et al. and U.S. Patent No. 6,271,565 to Hook et al.

2. Whether claims 15, 16, 19 and 24 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 5,688,700 to Kao et al. taken with U.S. Patent No. 6,190,980 to Yu et al. and U.S. Patent No. 6,271,565 to Hook et al, and further of U.S. Patent No. 5,597,752 to Niwa or U.S. Patent No. 5,434,093 to Chau et al.

3. Whether claim 18 is obvious under 35 U.S.C. §103(a) over U.S. Patent No. 5,688,700 to Kao et al. taken with U.S. Patent No. 6,190,980 to Yu et al. and U.S. Patent No. 6,271,565 to Hook et al, and further of U.S. Patent No. 4,495,220 to Wolf et al.

4. Whether claim 25 is obvious under 35 U.S.C. §103(a) over U.S. Patent No. 5,688,700 to Kao et al. taken with U.S. Patent No. 6,190,980 to Yu et al. and U.S. Patent No. 6,271,565 to Hook et al, and further of U.S. Patent No. 4,758,528 to Goth et al.

VII. GROUPING OF CLAIMS

The rejected claims do not all stand or fall together.

Claims 14-24 and 26 are patentable under 35 U.S.C. §112, second paragraph.

Claim 14 is an independent claim that is patentable over the prior art. Claims 15, 16, 17, 18, 20 and 24 stand or fall together with claim 14.

Claim 19 is patentable for reasons beyond the patentability of claim 14.

Claim 26 is patentable for reasons beyond the patentability of claim 14.

Claim 21 is an independent claim that is patentable over the prior art. Claims 22, 23 and 24 stand or fall with claim 21.

Claim 25 was cancelled in the amendment dated January 3, 2003.

VIII. ARGUMENT: ART OF RECORD DOES NOT ESTABLISH PRIMA FACIE CASE OF UNPATENTABILITY

A. The claims are patentable under 35 U.S.C. §112, second paragraph

Applicant believes that the claims are patentable under 35 U.S.C. §112, second paragraph. The Examiner rejected the claims as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner specifically references claims 14 and 21 as unclear, confusing and indefinite. The Examiner compares the language of claim 14 to the language of claim 21 to make this rejection. In particular the Examiner states that the rejection is based on calling different layers the "first layer" in two independent claims. The Examiner refers to of claim 14 reciting "forming an opening extending through said first layer..." and claim 21 reciting "forming an opening...and not through said first layer..." A related example, as Examiner points out as being inconsistent, is that claim 14 recites "forming a second layer in the gap..." and claim 21 recites "forming a fourth layer in the gap..." Applicant strongly disagrees with this rejection.

Claims 14 and 21 are both independent claims and are to be read as such. Referencing a layer as "first layer" in claim 14 has no bearing on the interpretation of the term "first layer" in claim 21.

Within claim 14, the layer referred to as "the first layer" includes layer 52 as shown in Figures 3-6 of the present application. The term "first layer" is used because this is the initial layer recited in the claim. It would not make sense to use "second" or "third" to indicate the layer when a first or second layer had not been previously introduced. As the Examiner can appreciate, the invention can be made without having the layer 44 or the layer 48 as the first layer on the substrate since these are preparation layers which are present in one embodiment but are not required to be present in all embodiments. Applicant has therefore made an effort to claim the invention in such a way as to cover those processes where preparation layers are not

formed. A person of skill in the art, reading claim 14, would clearly understand reference to the first layer as being a first layer for claim 14. Applicant could have referred to this layer as "an insulation layer" or "layer for which an opening is to be formed therein" or another name other than "first layer"; however this may create more confusion for the reader. Use of "first layer" seems the clearest.

Claim 21 is also believed sufficiently clear making references to "first layer" and "second layer." Within claim 21, the first layer corresponds to layer 48 or a combination of 48 and 44 and the second layer corresponds to layer 52. Within claim 21, additional layers are previously introduced and therefore the layer which has the opening is the "second layer." It is therefore believed that claim 21 is also sufficiently clear that a person of ordinary skill in the art, reading the claim, will understand the invention.

The standard of 35 U.S.C. § 112, second paragraph, is that the "claims particularly pointing out and distinctly claiming the subject matter which Applicant regards as his invention." The claims do this. Claim 14 makes clear what happens to the first layer and how the first layer is treated throughout the claim. The specification also supports this reading of claim 14. Similarly, claim 21 distinctly claims the subject matter of the invention of claim 21.

In making the rejection, the Examiner combined both claims 14 and 21. It appears the Examiner is willing to admit that claim 14 is clear on its face. Similarly, that claim 21 is clear on its face. It was only when the Examiner combined the claims that the Examiner was able to make the rejection. This is improper. Claim 14, in light of the specification, is clearly understandable and definite within itself. Similarly, claim 21 is distinct within itself. This is what the statute requires and the claims meet this standard.

In making the rejection the Examiner also had a reference to new matter. In particular the Examiner stated that "using different terms to recite the same layer rending the meaning and scope of the claims, if not new matter, being unclear,...." Applicant's attorney believes the claims do not represent new matter. The language in claim 14 the Examiner refers to was part of original claim 14. In particular, the reference to "first layer" is the same in current claim 14 as in claim 14 as originally filed. In addition, claim 21 clearly has basis in the original application as

filed. Accordingly, it is not believed that a new matter rejection is proper for either claim 14 or claim 21.

If the Examiner believes that a new matter rejection is proper, he is specifically requested to clearly state that the rejection is being made on new matter since the Examiner's off-hand reference to new matter is not clearly understood whether this is the basis for the rejection or not. To the extend it is a basis for the rejection, Applicant clearly disagrees and believes that new matter has not been inserted into any claim.

In the final rejection, the Examiner responded to Applicant's remark that the prior ground of rejection under 35 U.S.C. § 112 was still proper. Applicant had pointed out that a person in the art will read claim 14 of the patent without trying to also read all the language claim 21 into claim 14. And, if questions arise, they can read the file history of which these statements are a part. The Examiner maintained the rejection stating that the claims were confusing when read in light of each other, even in light of the specification. Applicant strongly disagrees. The claims are not the least bit confusing whether read alone, together or in light of the specification.

B. The claims are patentable over Kao taken with Yu and Hook.

Applicant believes that the claims are patentable over the teachings of Kao taken with Yu and Hook because even if combined, these references do not teach the claimed invention.

Independent claim 14 contains the following salient feature: "implanting ions into the substrate at a location beneath the dielectric spacers, the implanting being performed at an angle to provide implanted ions under the dielectric spacers on each side of the opening;..." An analogous feature of claim 21 is as follows: "implanting ions into the substrate at a location beneath the opening, the implanting being performed at multiple angles to provide implanted ions under the dielectric spacers on each side of the opening;..." Likewise, dependent claim 26 provides for implanting the ion at multiple angles. The specification, on page 7, lines 21-24, provides support for this feature stating "the self-aligned channel 81 is formed by implanting at multiple angles to provides "halos" or "pockets" of implanted ions under the dielectric spacers 74 on each side of the openings 56 but not in the gap 76 between the dielectric spacers 74 within the openings 56." The above feature is clearly not present in the combination of Kao as taken with Yu and Hook.

In the prior art, a reduced-size field effect transistor ("FET") can be formed by laying a material within an opening in a substrate and etching the material to form sidewall spacers within the opening. This method creates an opening with a width smaller than was previously possible. The resulting semiconductor can be seen in Figures 8 and 9 of U.S. Patent No. 5,688,700 to Kao et al., (Kao '700) of record as cited by the Examiner. To create a channel under the now-created gate, ion-implantation and annealing are conducted to form an LDD region with an opposite type material at the core as seen in Figure 10 of Kao, '700.

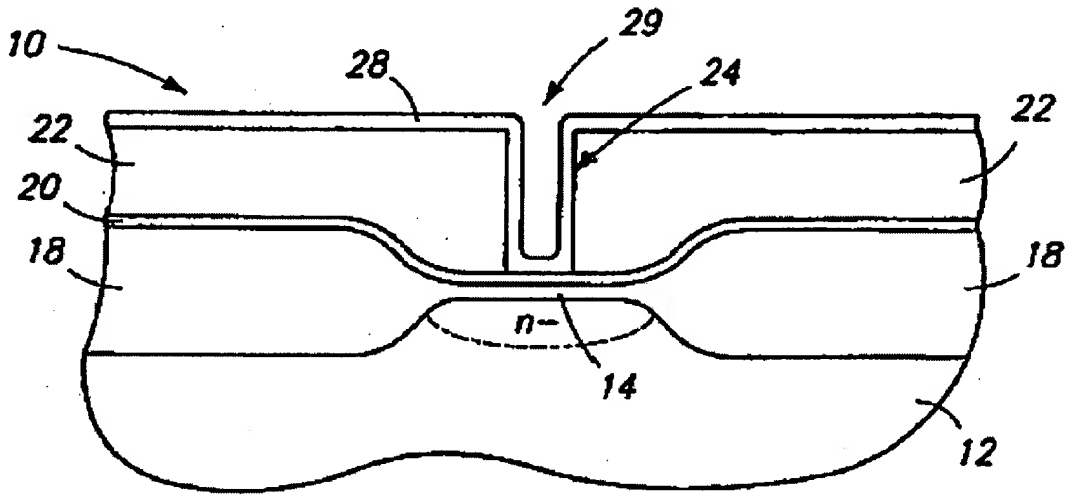


Figure 4 is a copy of Figure 8 from Kao '700

As can be seen by viewing Figure 4 above, a second layer of material 28 is provided over a first layer 22 at a thickness less than one-half the opening width 24 to define a narrower internal opening 29.

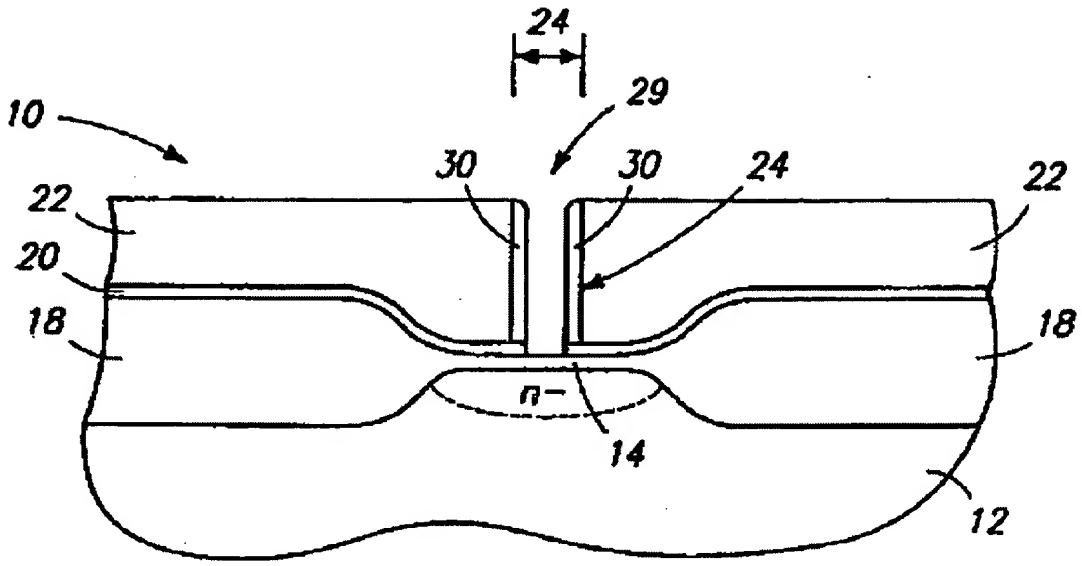


Figure 5 is a copy of Figure 9 from Kao '700

Figure 5 above demonstrates the resulting semiconductor after anisotropically etching the second layer from the first everywhere except within the first opening. This results in sidewall spacers 30 separated by opening width 29, the width of which is smaller than was previously possible.

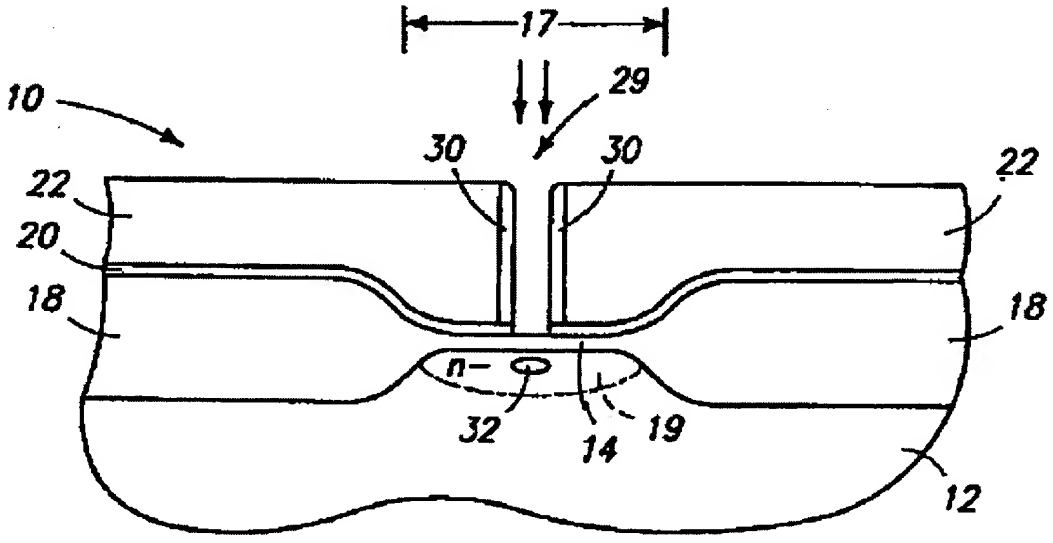


Figure 6 is a copy of Figure 10 from Kao '700

Figure 6 shows that a first LDD region 19 and a second core region 32 are implanted into the substrate beneath the opening 29 and sidewall spacers 30. Kao provides for implanting the

inner region 32 using the sidewall spacers 30 as a mask, thus requiring the implant region 32 to reside completely below the opening 29. It is critical in Kao that the implant region 32 *not* reside below the sidewall spacers 30 because the first LDD region 19 is of a different type (n-type of p-type) and maintains its physical boundary distinct from the second implant region 32. Further, the implant region 32 will likely be doped at a concentration larger than the LDD region 19 concentration.

The precise location of an implant region plays an important role in the performance of a FET. As seen in Figure 6 of U.S. Patent No. 6,190,980 to Yu et al., of record as cited by the Examiner, pocket and halo implant regions can be created by implanting the ions at an angle.

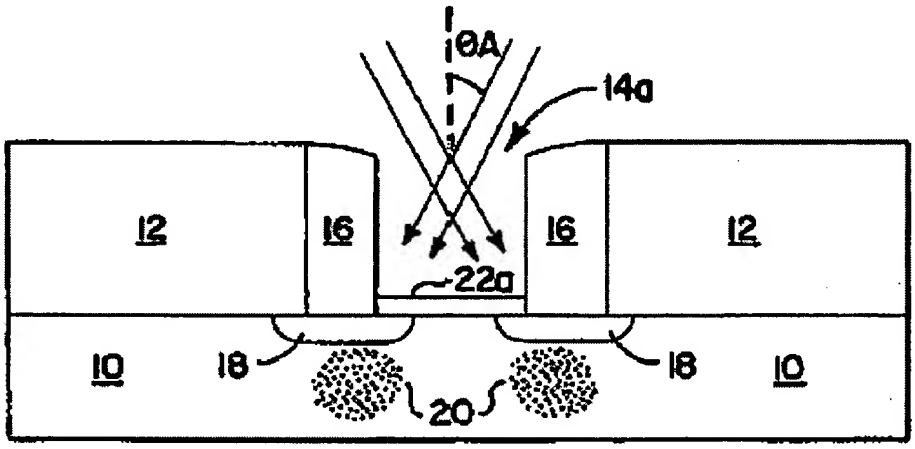


Figure 7 is a copy of Figure 3 from U.S. Patent No. 6,190,980, cited by the Examiner in this case.

Figure 7, above, shows the creation of pocket and halo extensions 20 within the substrate 10 below the nitride spacers 16. The depositing of the nitride spacers 16 and sacrificial oxide layer 22a allow the small-angle tilted implant that creates the self aligned pocket and halo extensions 20.

The Yu '980 patent cannot be used to supply the missing teachings of the Kao '700 patent. The Yu '980 patent deliberately selects a very small angle, namely an angle near 90° as according to Yu. This small angle ensures that a large amount of the implant will be in the window itself, namely within what has become the channel region. As can be seen by Figure 7 above, the implant will result in substantial overlap into the channel itself. There is no teaching

that the implant is to be placed only under the dielectric spacers as occurs in the present invention and not within the channel 76.

The Hook '565 patent fails to cure the missing features of the Yu '980 and Kao '700 patents. In particular, Hook '565 teaches an asymmetrical implant and that the implant is to be done within the main portion of the channel region. Indeed, he selects an implant angle which will place the ions underneath the gate electrode and will not place the ions underneath the barrier on either side. Rather, he uses the barrier 18 as a shield to prevent ions from being implanted underneath the sidewall on a particular side.

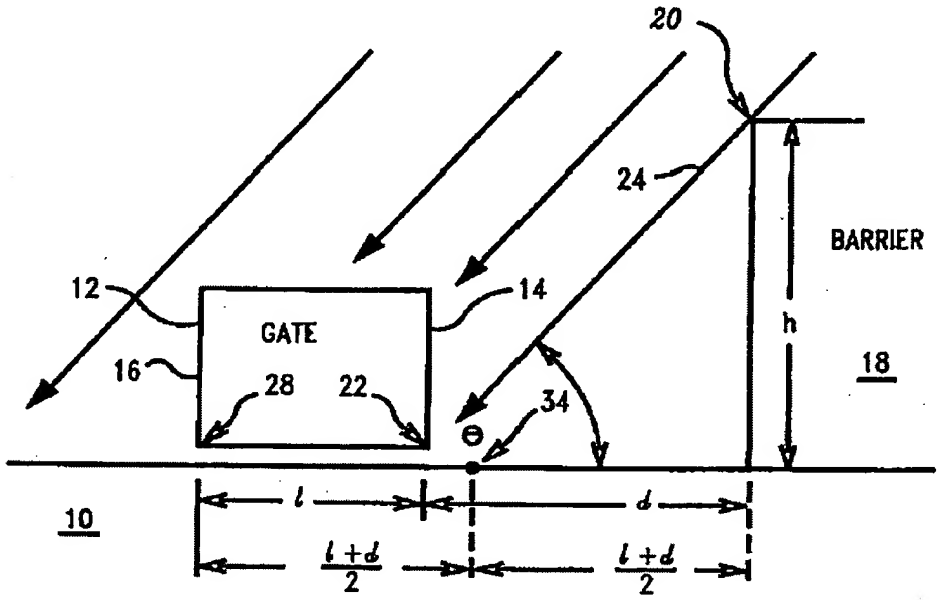


Figure 8 is a copy of Figure 2 from U.S. Patent No. 6,271,565, cited by the Examiner in this case.

Figure 8, above, shows an alternative method of implanting ions at an angle, in this case producing an asymmetrical semiconductor. Because implantation of an LDD region degrades semiconductor performance by increasing series resistance and overlap capacitance. Hook states that it is desirable to implant the lightly doped LDD region only on the drain side of the device to mitigate hot carrier degradation. Similarly, Hook states that it is desirable to implant a halo only on the source side of the gate. The Hook '565 creates such an asymmetrical semiconductor by using a barrier 18 to limit the location of implanted ions within the substrate. An ion stream 26 is blocked by the barrier 18 whenever its ion stream shadow strikes corner 22 of the gate. This

ensures that desired ion implantation location is achieved. Of course, the barrier 18 is placed between the side 16 of the gate and a distance d away from the side 14 of the gate. Simple geometry dictates the angle of implantation according to the Hook '565 invention.

Key reason, and yet further consideration that the claims are patentable over the combination at the Kao taken with Yu and Hook is that it is not possible to combine the teachings of these references while maintaining the functionality at the core of Kao. According to the techniques of Kao, the sidewall spacers are used as a mask to ensure that the implant region resides below the opening, or gate region. If Kao were to be modified by Yu and Hook by implanting the inner region at an angle, the LDD region and implant region would run together and retain no distinction. It is a fundamental characteristic of functioning FET's to have a separate n-type and p-type regions within the substrate, and combining Yu and Hook with Kao will disturb this critical feature. Therefore, we are left with a semiconductor with an internal implant region doped at a very high concentration and residing directly below the opening. A wider LDD region of opposite doping type surrounds this internal implant region.

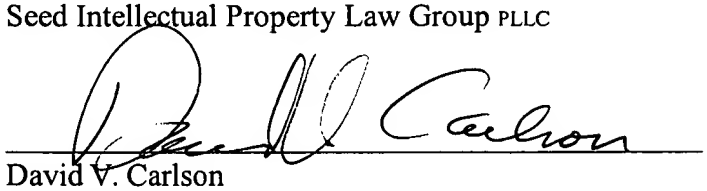
It is not possible to advance upon Kao with the teachings of Yu and Hook to implant ions at an angle to form pockets or halos under the dielectric spacers on each side of the opening. Kao teaches a first blanket implant to produce the LDD region 19 into active area region 17. Implanting ions into the entire active area has a particular effect on the substrate below the gate and dielectric spacers. In some circumstances, it is desirable to have this LDD implant into certain portions of the active area, which is not taught by Kao. In Figure 6 herein, Kao teaches the implant of V_t (of different doping type than the LDD region 19, and same doping type as source/drain 42 44) into the active area region 17 through the opening 29, using sidewall spacers 30 as a mask, to create an implant region 32 which does *not* reside under sidewall spacers 30. The functionality of the semiconductor in Kao would be upset by implanting this second set of ions under the sidewall spacers 30. If the second ion implants were to be inserted under the sidewall spacers 30, the source and drain 42, 44 would be directly connected via implant region 32, of the same doping type. This would link together the source and drain, thereby defeating the entire point of the FET channel and leading to a failure in the semiconductors performance.

Yu and Hook both teach the implantation of ions at an angle to produce implant regions under the sidewall spacers. Figure 7 herein of in Yu depicts pocket 20 which has been implanted beneath nitride spacers 16. Likewise, Figure 8 herein from Hook shows the implantation of ions at an angle to produce a LDD region 44 and halo region 46 beneath sidewall spacers 50, 52, as shown in Figure 3. The teachings of Yu and Hook are not available to advance on Kao because they implant ions beneath sidewall spacers. As discussed in the paragraph above, implanting ions beneath the sidewall spacers in Kao would disrupt the functionality of the FET by creating a link directly between the source and drain. Therefore, claim 14, 21 and 26 are patentable over the combined teachings of Kao, with Yu and Hook.

IX. CONCLUSION

In summary, applicant believes that the claims of the present invention are patentable, and not obvious in light of the combination of the cited references made by the Examiner. Allowance of the claims is respectfully requested.

Respectfully submitted,
Seed Intellectual Property Law Group PLLC



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APPENDIX A

X. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

14. (Previously Presented) A method of forming a feature having a critical dimension comprising:

providing a substrate;

forming a first layer having a first thickness;

forming an opening extending through the first layer, the opening having vertical sidewalls separated by a width greater than the critical dimension;

forming a blanket dielectric layer having a second thickness in the opening, on the first layer and on the sidewalls, the second thickness being half or less of the first thickness;

selectively and anisotropically etching the blanket dielectric layer to form dielectric spacers on the sidewalls and to remove the blanket dielectric layer from a bottom of the opening without etching the first layer, the dielectric spacers separated by a gap having a width equal to the critical dimension;

implanting ions into the substrate at a location beneath the dielectric spacers, the implanting being performed at an angle to provide implanted ions under the dielectric spacers on each side of the opening;

forming a second layer in the gap and on the first layer;

removing those portions of the second layer formed on the first layer using a chemical-mechanical polish without removing portions of the second layer in the gaps; and

removing the first layer but not the dielectric spacers.

15. (Original) The method of claim 14 wherein forming a first layer comprises forming a series of chemically distinct layers on the surface of the substrate, a top one of the series of layers having the first thickness, the first thickness being five thousand Angstroms or less.

16. (Original) The method of claim 14 wherein forming a first layer comprises:

forming a thermal oxide on the substrate, the substrate formed from silicon;

forming a silicon nitride layer having a thickness of less than five hundred Angstroms on the thermal oxide; and

forming a silicon dioxide layer having the first thickness on the silicon nitride layer, the first thickness being five thousand Angstroms or less.

17. (Original) The method of claim 14 wherein forming a blanket dielectric layer comprises forming a blanket dielectric layer of silicon nitride.

18. (Original) The method of claim 14 wherein forming a blanket dielectric layer comprises forming a blanket dielectric layer of silicon nitride using LPCVD.

19. (Original) The method of claim 14, wherein the substrate comprises silicon and forming a second layer in the gap and on the first layer comprises:

pre-gate cleaning;

thermally growing a gate oxide on the substrate within the gap;

forming a channel within the gap;

forming the second layer of conductive material; and

chemical-mechanical polishing to remove the second layer from the first layer.

20. (Original) The method of claim 14 wherein forming the second layer comprises forming the second layer of polycrystalline silicon.

21. (Previously Presented) A method of forming a feature having a selected dimension comprising:

forming a first layer having a first thickness on a semiconductor substrate;

forming a second layer over said first layer, said second layer having a second thickness thicker than said first layer and being etchable by a different etch chemistry than said first layer;

forming an opening having vertical sidewalls separated by a width greater than said selected dimensions, said opening extending through said second layer and not through said first layer;

forming a blanket dielectric layer having a third thickness on the second layer and within the opening and on top of the first layer within the opening, said blanket dielectric layer being on the sidewalls of the second layer, the third thickness being half or less that of the second thickness;

selectively and anisotropically etching the blanket dielectric layer to form dielectric spacers on the sidewalls of the second layer and to remove the blanket dielectric layer from a bottom of the opening;

implanting ions into the substrate at a location beneath the opening, the implanting being performed at multiple angles to provide implanted ions under the dielectric spacers on each side of the opening;

etching the first layer to expose the substrates and form a gap having a width equal to the selected dimension between the dielectric spacers;

forming a fourth layer in the gap and on the substrate; and

removing any remaining portions of the second layer without removing the dielectric spacers.

22. (Original) The method of claim 21 wherein forming a first layer comprises forming two chemically distinct sub-layers on the surface of the substrate, each being selectively etchable with respect to the other, the combined sub-layers comprising the first layer having the first thickness.

23. (Original) The method of claim 21 wherein forming a first layer comprises:

forming a thermal oxide on the substrate, the substrate formed from silicon;

forming a silicon nitride layer having a thickness of less than five hundred Angstroms on the thermal oxide.

24. (Original) The method according to claim 21 wherein said second layer is formed of silicon dioxide having a thickness of approximately five thousand Angstroms.

26. (Previously Presented) The method according to claim 14 wherein the implants are performed at multiple angles.

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